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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/776,541	02/10/2004	Amir Morad	13757US03	3126

23446 7590 06/10/2010

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EXAMINER	
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ART UNIT	PAPER NUMBER
2621	

MAIL DATE	DELIVERY MODE
06/10/2010	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/776,541	MORAD ET AL.	
	Examiner	Art Unit	
	Tung Vo	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/30/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02/10/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 10-20 and 24-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250).

Re claims 10 and 24, Adolph discloses a audio/video encoder device (fig. 3, a single device) comprising, on a single integrated circuit:

multiplexer circuitry (EMUX of fig. 3) that operates in a first mode (MMUX of fig. 3, the performing of MMUX is considered as the first mode) and a second mode (MUX1 and MUX2 of fig. 3, the performing of MUX 1 and MUX 2 are considered as the second mode),

which when operating in the first mode (MMUX of fig. 3) produces a first multiplexed stream from first compressed video (VE1 of fig. 3), first compressed audio (AE1 of fig. 3), second compressed video (VE2 of fig. 3), and second compressed audio (AE2 of fig. 3); and

which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3);

a first encoder (VE1 and AE1 of fig. 3) that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;

a second encoder (VE2 and AE2 of fig. 3) that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;

wherein the device (fig. 3) transmits the first multiplexed stream (the output of MUX1, MUX1 of fig. 3)) to circuitry external (fig. 4) to the device (fig. 3) via a first output of the device (MOD and BBRF of fig. 3, transmitting the first output of the device (fig. 3)); and

wherein the device (fig. 3) transmits the second multiplexed stream (the output of MUX2, MUX2 of fig. 3) to circuitry external (fig. 4) to the device (fig. 3) via a second output of the device (MOD and BBRF of fig. 3, transmitting the second output (the output of MUX2) to the DMUX of fig. 4).

It is noted that Adolph does not particularly teach a single chip comprises the multiplexer, encoders, and control circuitry that synchronizes the multiplexing circuitry, the first encoder, and the second encoder as claimed.

Hinchley teaches a single chip (120 of fig. 1) comprises the multiplexer (204 of fig. 2), encoders (208 of fig. 2), and control circuitry (250 of fig. 2) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder (212, 214, 216, 218, and 220 of fig. 2).

Taking the teachings of Adolph and Hinchley as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Hinchley into the system of Adolph to

efficiently multiplex the incoming streams together and flexible to adjust the data rate for different formats.

Re claim 11, Adolph further discloses wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder (VE1 and AE1, VE2 and AE2 of fig. 3).

Re claims 12 and 25, Adolph further discloses wherein the first encoder and the second encoder operate concurrently (VE1, AE1, VE2, and AE2 of fig. 3, in parallel).

Re claims 13 and 26, Adolph modified by Hinchley, Hinchley further teaches wherein the first encoder and the second encoder inherently perform luminance and chrominance filtering *(note MPEG-1 and MPEG-2 video/audio compression standards. Hence, a data block represents a macroblock, which is a sixteen by sixteen matrix of luminance pixels and two, four or eight, by eight matrices of chrominance pixels as defined by MPEG standards, wherein luminance and chrominance are 4:2:0, 4:2:2, or 4:4:4 as shown in Hinchley, col. 3, lines 30-38).*

Re claims 14 and 27, Adolph modified by Hinchley, Hinchley further wherein the device comprises at least one interface (122 of fig. 1) for direct connection to external memory devices (108 and 116 of fig. 1) used as one or both of a frame buffer and/or an output buffer for compressed data.

Re claims 15 and 28, Adolph modified by Hinchley, Hinchley further teaches wherein the device comprises at least one bus interface (122 of fig. 1) that is configurable to operate to couple the control circuitry (250 of fig. 1) and at least one controller external (104 of fig. 1) to the device,

wherein the at least one bus interface (122 of fig. 1) comprises inherently a plurality of separate electrical signals *(note each of the components inherently has its own electrical signal*

(e.g. electron, voltage, digital data). Figure 1 of Hinchley has a plurality of separate electrical elements that inherently have a plurality of separate electrical signals. It is further noted that the specification of the present invention does not particularly disclose a plurality of separate electrical signals, so the plurality of electrical signals are understood that each element has its own electrical signal as shown in fig. 1 of Hinchley, e.g. the integrated multimedia encoding system has its own electrical signal (e.g. encoded data, uncompressed data ...)).

Re claims 16 and 29, Adolph modified by Hinchley, Hinchley further teaches wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface *(Note Hinchley teaches the unified memory module 204 receives the adjusted elementary streams 216, 218, the output combined data 224 as well as data streams from other data sources 236, such as from the PCI bus, through a conventional FIFO 244).*

Re claims 17 and 30, Adolph modified by Hinchley, Hinchley further teaches wherein the at least one bus interface is configurable to act as a bus master (122 of fig. 1) inherently using direct memory access *(support by Larson, US 5,821,987, the vision processor 48B preferably incorporates a DMA data interface with a zero-run/amplitude encoder/decoder, fig. 1).*

Re claims 18 and 31, Adolph modified by Hinchley, Hinchley further teaches wherein the at least one bus interface (122 of fig. 1) enables transfer of one or both of uncompressed audio data and/or video data for processing by the device.

Re claims 19 and 32, Adolph modified by Hinchley, Hinchley further teaches wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions *(e.g. 104 of fig. 1; note the computer system 100 has a central processing unit 104, which may execute specific programs related to multimedia processing; wherein a program inherently has*

microcode instructions, e.g. 606 of fig. 6; col. 5, lines 25-65) received by the device via the at least one bus interface (122 of fig. 1, PCI bus).

Re claims 20 and 33, Adolph further wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels (V1, A1, V1, and A2 of fig. 3).

3. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250) in view of Ishihara et al. (US 6,516,031).

Re claims 21-22 and 34-35, Adolph modified by Hinchely, Adolph and Hinchley further teaches the MPEG-2 encoder (208 of fig. 2 of Hinchley) that would obviously has motion estimation except a plurality of search processors for performing motion analysis in parallel, each upon a different portion of a macroblock as claimed.

However, Ishihara teaches a plurality of search processors (7 of fig. 2) for performing motion analysis in parallel, each upon a different portion of a macroblock (PE1, PE2….PE33 of fig. 7; e.g. fig. 13).

Taking the teachings of Adolph, Hinchley, and Ishihara as a whole, it would have been obvious to one of ordinary skill in the art to modify the processor array (7 of fig. 2) of Ishihara into the motion estimation of the combination of Adolph and Hinchley to provide an improvement for reducing a hardware volume.

4. Claims 23 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adolph et al. (US 5,825,430) in view of Hinchley et al (US 6,490,250) and Ishihara et al. (US 6,516,031), and further in view of Kopet et al. (US 5,448,310).

Re claim 23, the combination of Adolph, Hinchley, and Ishihara further teaches wherein the plurality of search processors operates in parallel upon a single macroblock (e.g. figs. 9 and 10 of Ishihara) and suggests the processor performs half pixels search, except each search processor operating at a different one of a plurality of resolutions as claimed.

However, Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29).

Taking the teachings of Adolph, Hinchley, Ishihara, and Kopet as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Adolph, Hinchley, and Ishihara in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

5. Claims 10-12, 15-16, 20, 24-25, 28-29, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430).

Re claims 10 and 24, Krishnamurthy teaches a single-chip audio/video encoder device (fig. 3) comprising, on a single integrated circuit (fig. 3, note two and more different sub-system could be implemented on a single board, col. 20, lines 34-42):

multiplexer circuitry (308 of fig. 3) that operates in a first mode and a second mode (col. 20, lines 22-25, "multi-channel mode" would obviously suggest a first mode and a second mode), which when operating in the first mode (308 of fig. 3, the multiplexer (308) for multiplexing up to 24 different channels of transport bitstreams from the MPEG-2 encoders; col. 20, lines 10-11) produces a first multiplexed stream (fig. 5, multiplexing bitstreams and outputting a first multiplexed bitstream) from first compressed video (320 of fig. 3), first compressed audio (322 of fig. 3), second compressed video (ENCn, 320 of fig. 3), and second compressed audio (ENCn, 322 of fig. 3); and

a first encoder (306 of fig. 3) that receives first uncompressed video data and first uncompressed audio data, and that produces the first compressed video and the first compressed audio;

a second encoder (306 of fig. 3, ENCn) that receives second uncompressed video data and second uncompressed audio data, and that produces the second compressed video and the second compressed audio;

control circuitry (304 of fig. 3, note the CPU (304) is programmable to control all elements, so the CPU would obviously synchronize all element as described in figure 3) that synchronizes the multiplexing circuitry, the first encoder, and the second encoder;

wherein the device (fig. 3, see also fig. 5) transmits the first multiplexed stream to circuitry external (506 of fig. 5, col. 20, lines 27-28) to the device via a first output of the

device; and wherein the device (fig. 5) transmits the second multiplexed stream to circuitry external (506 of fig. 5; col. 20, lines 27-28) to the device via a second output of the device.

Krishnamurthy does not particularly teach **when operating in the second mode** concurrently produces the first multiplexed stream from the first compressed video and the first compressed audio, and produces a second multiplexed stream from the second compressed video and the second compressed audio as claimed.

Adolph teaches which when operating in the second mode (MUX1 of fig. 3) concurrently produces the first multiplexed stream (the output of MUX1) from the first compressed video (VE1 of fig. 3) and the first compressed audio (AE1 of fig. 3), and produces a second multiplexed stream (MUX2 of fig. 3, the output of MUX2) from the second compressed video (VE2 of fig. 3) and the second compressed audio (AE2 of fig. 3).

Taking the teachings of Krishnamurthy and Adolph as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Adolph into the system of Krishnamurthy to reduce the perceptibility of errors and picture failures during the terrestrial reception of the signals.

Re claim 11, Krishnamurthy further teaches wherein the first encoder and the second encoder each comprise a video encoder and an audio encoder (306, 320, and 322 of fig. 3; ECNn of fig. 3).

Re claims 12 and 25, Krishnamurthy further teaches wherein the first encoder and the second encoder operate concurrently (parallel encoding, 306 of fig. 3).

Re claims 15 and 28, Krishnamurthy further teaches wherein the device comprises at least one bus interface (PCI, 302 and 310 of fig. 3) that is configurable to operate to couple the

control circuitry (304 of fig. 3) and at least one controller external (316 of fig. 3, downloading micro-codes for MPEG-2 encoder chip, 306 of fig. 3, col. 19, lines 22-28) to the device, wherein the at least one bus interface comprises a plurality of separate electrical signals (PCI of fig. 3).

Re claims 16 and 29, Krishnamurthy further teaches wherein the at least one bus interface is configurable as a peripheral component interconnect (PCI) bus interface (302, PCI BUS of fig. 3).

Re claims 20 and 33, Krishnamurthy further teaches wherein each of the first uncompressed audio data and the second uncompressed audio data represent two audio channels (AUDIO ENC of fig.3).

Re claims 18-19, 31-32, Krishnamurthy further teaches wherein the at least one bus interface enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

6. Claims 13 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430), and further in view of Bruck (US 6,519,289).

Re claims 13 and 26, Krishnamurthy does not particularly teach wherein the first video encoder and the second video encoder perform luminance and chrominance filtering.

However, Bruck teaches wherein the video encoder performs luminance and chrominance filtering (col. 1, lines 59-col. 2, line 8).

Taking the teachings of Krishnamurthy, Adolph, and Bruck as a whole, it would have been obvious to one of ordinary skill in the art to modify the luminance and chrominance filtering of Bruck into Krishnamurthy and Adolph to improve the picture quality.

In response to the applicant arguments filed on 06/10/2008, the applicant argues that Bruck fails to overcome the deficiencies of Krishnamurthy, page 23.

The examiner respectfully disagrees with the applicant. It is submitted that Krishnamurthy teaches the encoder (306 of fig. 3) for encoding video and audio stream based on the MPEG-2 standards, wherein the MPEG-2 standard would obviously have the luminance and chrominance filtering by Bruck (col. 1, lines 59-col. 2, line 8). Therefore, the combination of Krishnamurthy and Bruck make obvious the claimed invention.

7. Claims 14, 17-19, 27, 30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430) in view of Hinchley et al. (US 6,490,250).

Re claims 14, 17, 27, and 30 , Krishnamurthy does not particularly disclose external memory devices used as one or both of a frame buffer and/or an output buffer for compressed data; wherein the at least one bus interface is configurable to act as a bus master using direct memory access as claimed.

Hinchley teaches a first storage external to the device and a second storage external (108 and 116 of fig. 1) to the device (120 of figs. 1 and 2) and the at least one bus interface is

configurable to act as a bus master (122 of fig. 1) using direct memory access (Note the bus (122) would obviously be the PCI bus and/or direct memory access, which serves the same purpose of transferring and receiving data to and from components within the circuit (100 of fig. 1).

Therefore, taking the teachings of Krishnamurthy, Adolph, and Hinchley, it would have been obvious to one of ordinary skill in the art to incorporate the first and second storages and random access memory with the interface bus (108, 116, and 122 of fig. 1) of Hinchley into the first and second interface (318 of fig. 2) Krishnamurthy and Adolph to provide an integrated multimedia encoding system which operates with reduced memory storage requirements is also needed.

Re claims 18-19, 31-32, Krishnamurthy further teaches wherein the at least one bus interface (PCI BUS, 302 of fig. 3) enables transfer of one or both of uncompressed audio data and/or video data for processing by the device (318 of fig. 3); wherein the first encoder, the second encoder, and the multiplexer circuitry execute microcode instructions received by the device via the at least one bus interface ("C" programmable language and micro-codes are used to instruct elements in figure 3; col.18, lines 28-33; col. 19, lines 26-28).

8. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430), and further in view of Boice et al. (US 6,823,013).

Re claims 21-23, and 34-36, Krishnamurthy does not particularly disclose each of motion estimation processors comprises a plurality of search processors that operate in parallel upon a

single macroblock, and each search processor operating at a different one of a plurality of resolutions (scaling or half pixel search, quarter pixel search) as claimed.

Boice teaches each of motion estimation processors (52 of fig. 4) comprises a plurality of search processors (see Abstract: a consequence of the multiple processors subdividing the extended window and analyzing each subdivision in parallel) that operate in parallel upon a single macroblock (figs. 1 and 3), and each search processor operating at a different one of a plurality of pixels blocks (scaling or half pixel search, quarter pixel search, 36, 38, and 40 of fig. 3)

Therefore, taking the teachings of Krishnamurthy, Adolph, and Boice as a whole, it would have been obvious to one of ordinary skill in the art to incorporate the plurality of search processors (52 of fig. 4) of Boice into each of motion estimation processor of Krishnamurthy and Adolph to provide the process of motion estimation effectively reduces the temporal redundancy in successive video frames by exploiting the temporal correlation (similarities) that often exists between successive frames.

9. Claims 21-22 and 34-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krishnamurthy et al. (US 6,665,872) in view of Adolph et al. (US 5,825,430) and Boice et al. (US 6,823,013), and further in view of Kopet et al. (US 5,448,310).

Re claim 23, the combination of Krishnamurthy, Adolph, and Boice teaches wherein the plurality of search processors operates in parallel upon a single macroblock, except each search processor operating at a different one of a plurality of resolutions as claimed.

However, Kopet teaches the motion estimation coprocessor of the present invention provides improvements in performance over prior art devices. For example, the motion estimation coprocessor of the present invention may perform either full, exhaustive block matching searches or multiple step hierarchical searches to either full or half pixel search resolution (col. 2, line 50 –col. 3, line 29).

Taking the teachings of Krishnamurthy, Adolph, Boice, and Kopet as a whole, it would have been obvious to one of ordinary skill in the art to modify the teachings of Kopet into the combined motion estimation of Krishnamurthy Adolph, and Boice in order to improve system speed and performance over prior art devices through parallel performance of these tasks.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Boice et al. (US 7,072,393) discloses multiple parallel encoders and statistical analysis thereof for encoding a video sequence.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tung Vo whose telephone number is 571-272-7340. The examiner can normally be reached on Monday-Wednesday, Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on 571-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Tung Vo/
Primary Examiner, Art Unit 2621